REMARKS

I. Status of the Claims

Claims 1 - 10 have been examined and stand rejected on various grounds. Claim 11 has been added.

II. Objections to the Specification

The Office Action identified informalities in the specification regarding the method steps of original Figure 4. The amending of Figure 4 into Figures 4a and 4b addresses the noted informality.

III. Objections to the Drawings

Minor informalities regarding Figures 3 and 4 were identified in the Office Action, and have been corrected consistent with the amendments herein. Red-lined copies of the figures are attached, as is a Letter to the Draftsman.

IV. Objections to the Claims

The Office Action identified an improper acronym in claim 7. The appropriate language for the acronym has been amended into claim 7. Claim 10 has also been amended in this manner.

III. Rejections Under 35 U.S.C. §112, First Paragraph

The Office Action rejected claims 1, and 7-10, under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner identified the term "programmable delay circuitry", and the step "identifying" as not being described in the specification.

The Examiner is invited to review the specification on page 3, lines 10 - 12, amended page 5, line 6, and page 5, line 28. The applicants assert that the noted terms are well-known to those skilled in the art, and relate to subject matter that is described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention ***without undue experimentation***.

IV. Rejections Under 35 U.S.C. §103

The Office Action identified rejections to claims 1 - 10 under 35 U.S.C. §103 as being unpatentable over applicant's admitted prior art in view of Lopez (U.S. Patent No. 5,111,208), Catiller (U.S. Patent No. 4,429,389) and Conner (U.S. Patent No. 5,794,175).

To begin with, the Examiner's interpretation of the admitted prior art (APA) is innaccurate. As the Applicants admit again, the APA comprises a one-to-one correspondence between each tester channel and a programmable delay circuit (or deskew circuit). For semiconductor devices that employ 128 pins, 128 channels are typically employed to test the device, and a corresponding 128 deskew circuits allocated to the channels. To test eight of these devices in parallel, conventionally, 1024 channels are used, with 1024 deskew circuits employed.

The architecture claimed in claims 1 - 11 utilizes shared deskew circuits to minimize the costs associated with the tester. In other words, for example, one deskew circuits may be allocated among four channels. For moderate accuracy applications, the signal delays for each channel are determined, and the maximum range of delay calculated. An averaged compensating delay may then be programmed into the deskew circuit for use during test, and applied simultaneously to the four channels during test.

In a high accuracy mode, each deskew circuit is assigned to an individual channel, and the delay programmed for that specific channel during test. However, instead of testing all the devices simultaneously, as in the moderate accuracy mode, groups of channels (corresponding to groups of devices-under-test) are employed for a sequential test of the devices.

In this manner, low cost is achieved without compromising accuracy, resulting in a highly flexible and beneficial architecture.

While the Examiner's citation to Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966) is helpful, it is critical to understand that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Cited Art

The Lopez reference has no relevance to the field of automatic test equipment. This patent describes a beat frequency calibration scheme for scanning array antennas. The disclosure, as taught by Lopez, is intended for use "where multiple channels provide various time delays and/or phase shifts for steering a beam of radiation" (col. 1, lines 19-20). Automatic test equipment utilizes calibration circuitry to eliminate channel-to-channel delay ("de-skewing" literally means to remove skew).

While Lopez describes a beat frequency technique to fine-tune the desired phase shift between radiation steering channels, the APA on the other hand employs programmable delay circuits for each channel to eliminate channel-to-channel phase shift. There is no motivation to combine these references due to their fundamental differences.

As to Catiller, the reference deals with testing static PROMs and has no relevance to calibrating automatic test equipment for testing integrated circuits having pins for receiving signals at various timings.

Conner teaches the use of a separate deskew circuit for each channel, and is a good example of the conventional art, consistent with the applicant's admitted prior art. Combining Conner with any of the above references would motivate one skilled in the art to employ a separate deskew circuit per channel. This combination teaches away from using a shared deskew scheme as claimed in claims 1 - 11. Consequently, there would be no motivation to combine the references with Conner to arrive at a shared deskew scheme as claimed in claims 1 - 11.

For all of the above reasons, claims 1 - 11 are believed patentable over the cited art and reconsideration is respectfully requested.

Please charge a one-month extension fee of $110 and an additional independent claim fee of $86 to Deposit Account No. 20-0515.

Respectfully Submitted

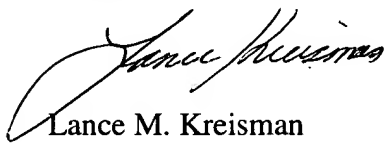

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FIG. 3

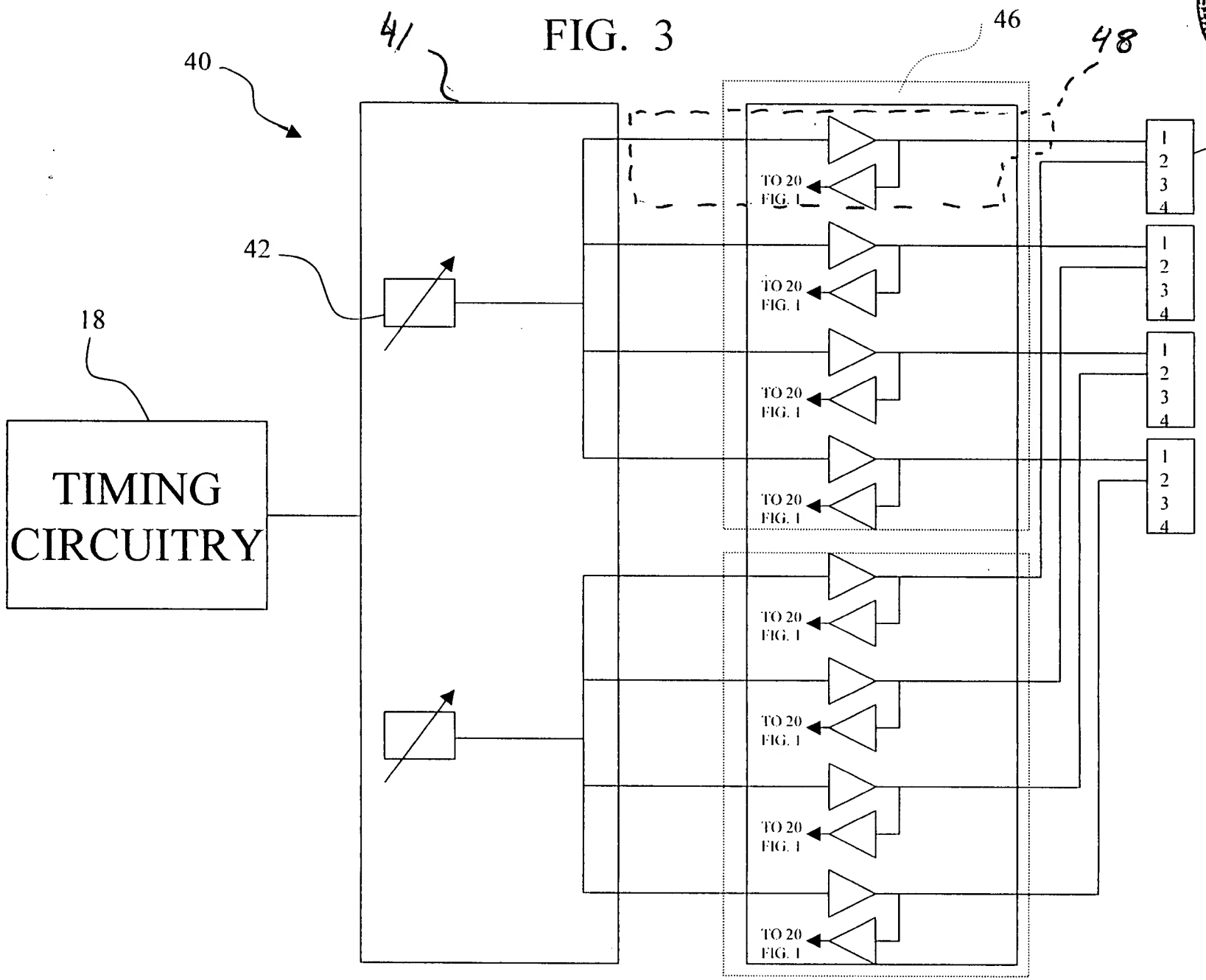

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FIG. 4a

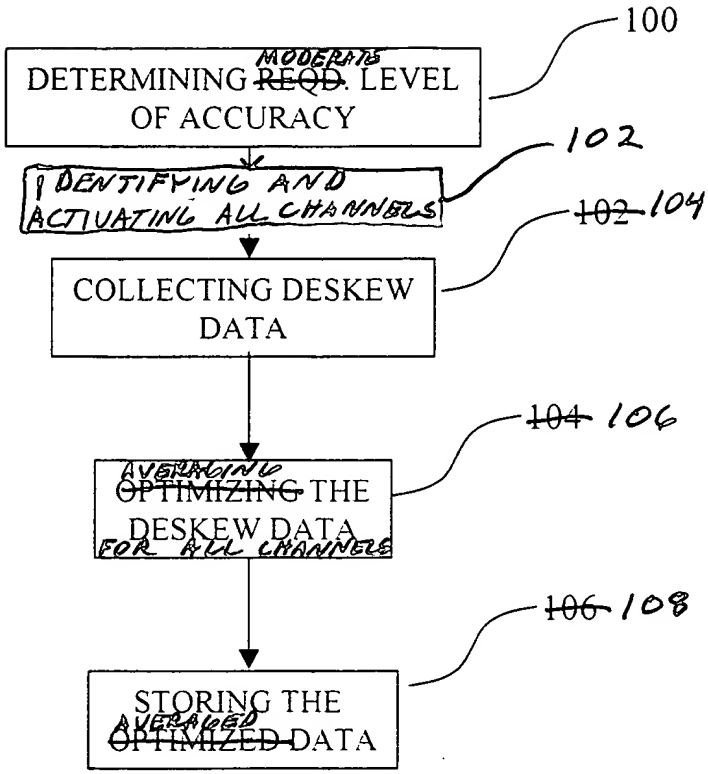
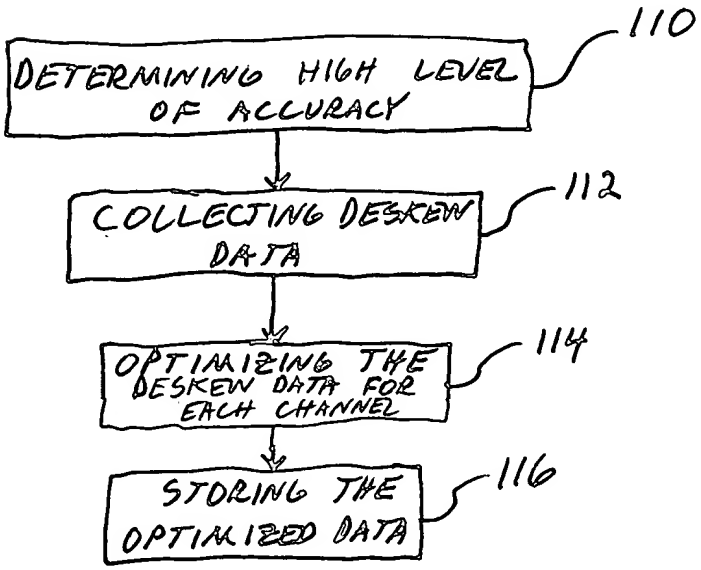


FIG. 4b



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